

Figure 1

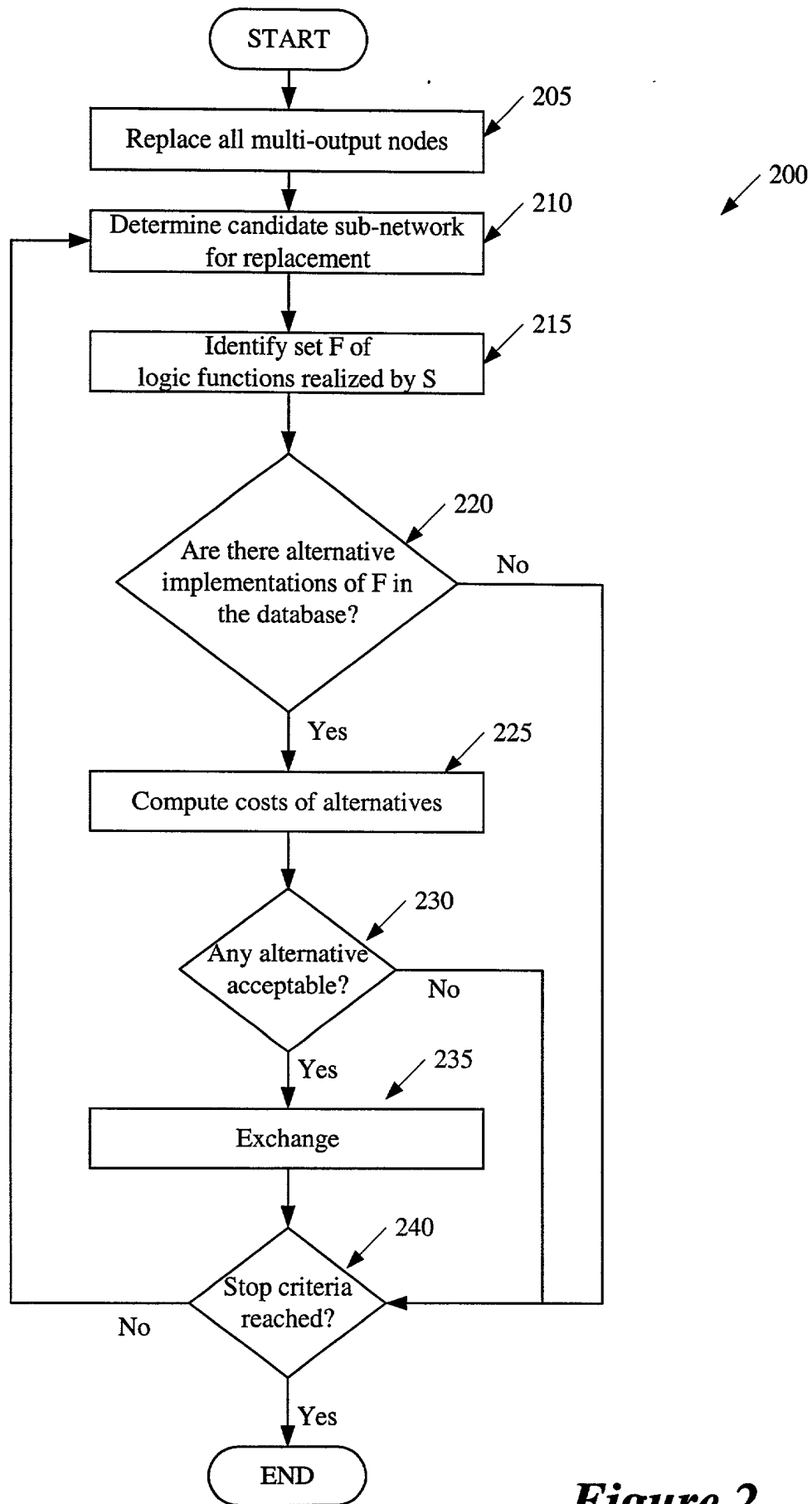


Figure 2

FIG. 3 is a schematic diagram of a logic circuit 300. The circuit 300 includes a first AND gate 310, a second AND gate 320, a third AND gate 325, a fourth AND gate 330, a fifth AND gate 305, a sixth AND gate 315, a seventh AND gate 335, and an eighth AND gate 340. The circuit 300 also includes a first OR gate 315, a second OR gate 320, a third OR gate 325, a fourth OR gate 330, a fifth OR gate 305, a sixth OR gate 315, a seventh OR gate 335, and an eighth OR gate 340. The circuit 300 is configured to receive inputs Y0, Y1, Y2, Y3, Y4, X0, X1, X2, X3, X4, X5, X6, and X7, and to produce outputs Y0, Y1, Y2, Y3, Y4, X0, X1, X2, X3, X4, X5, X6, and X7.

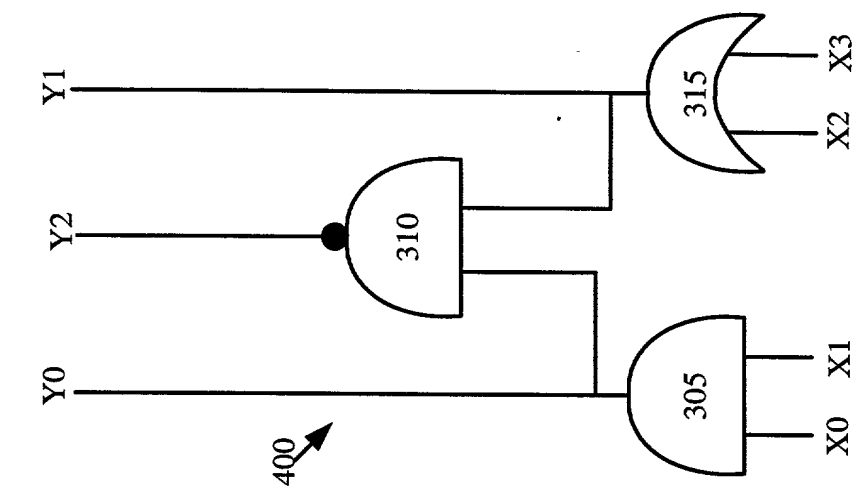


Figure 4

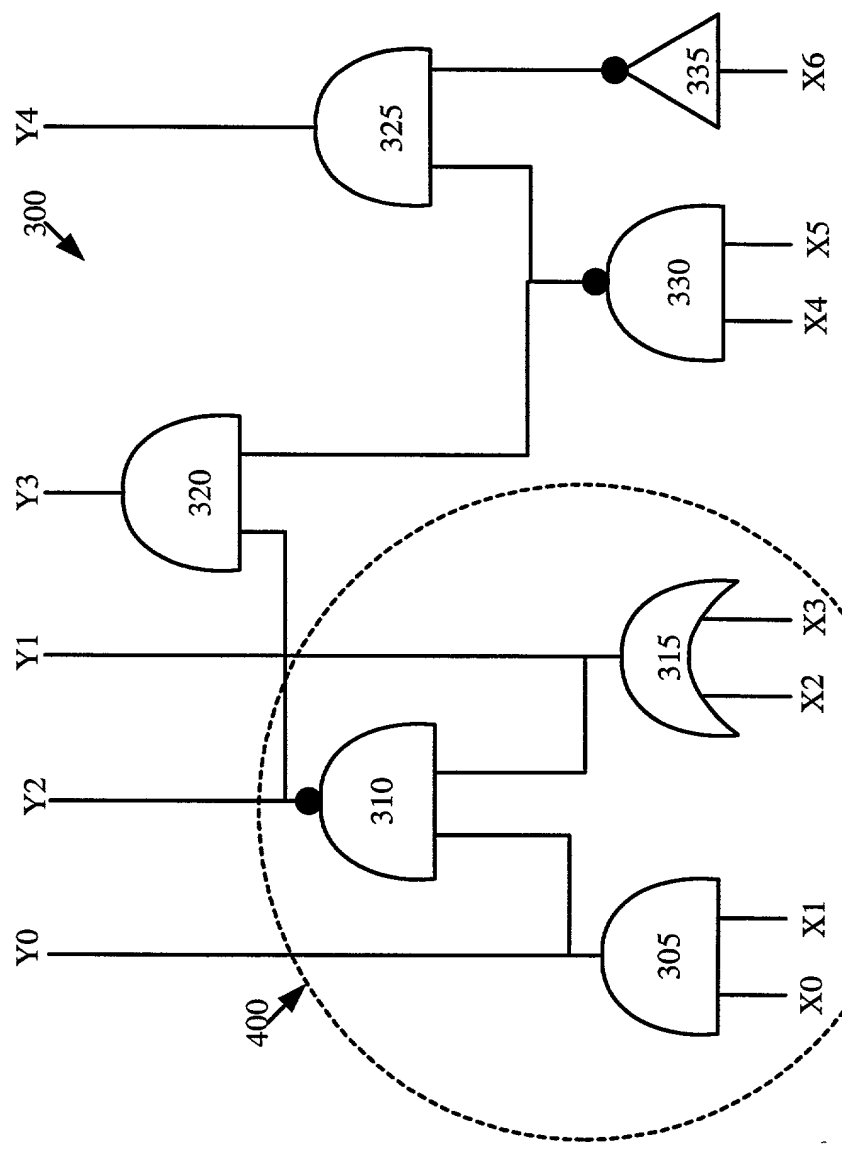


Figure 3

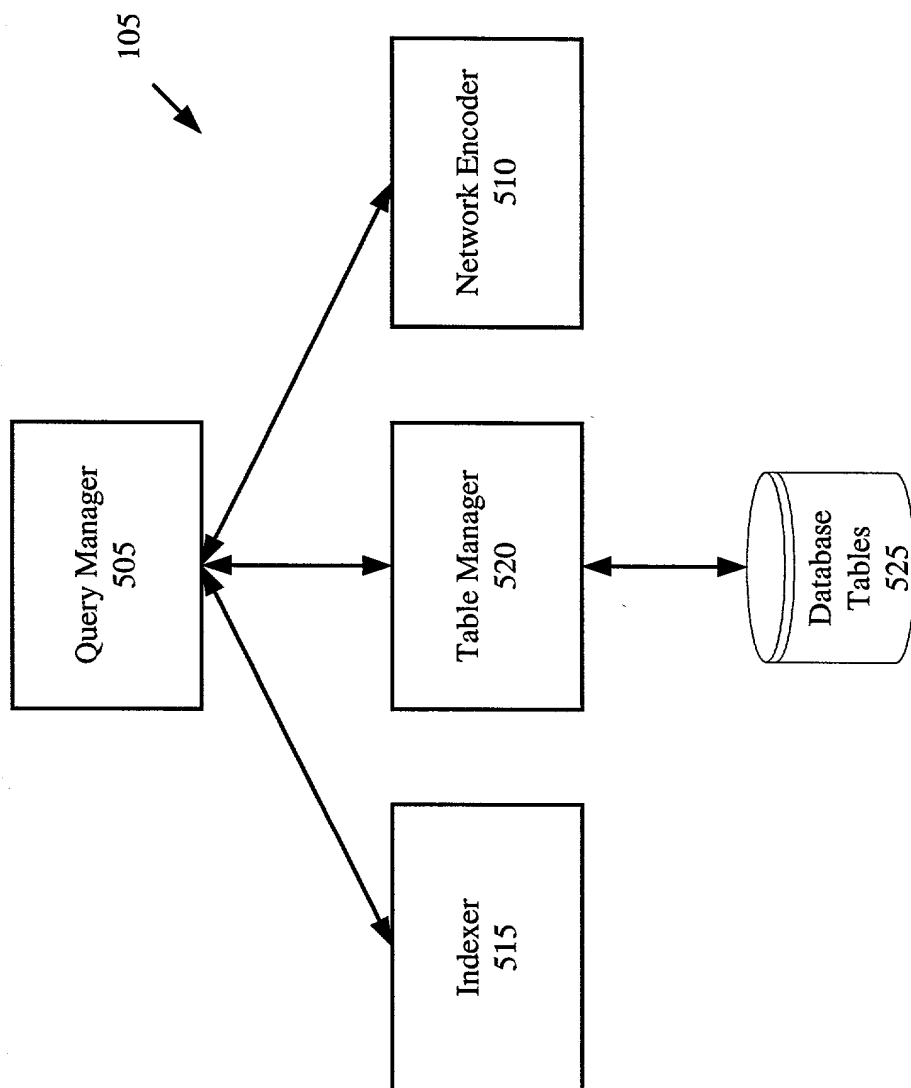


Figure 5

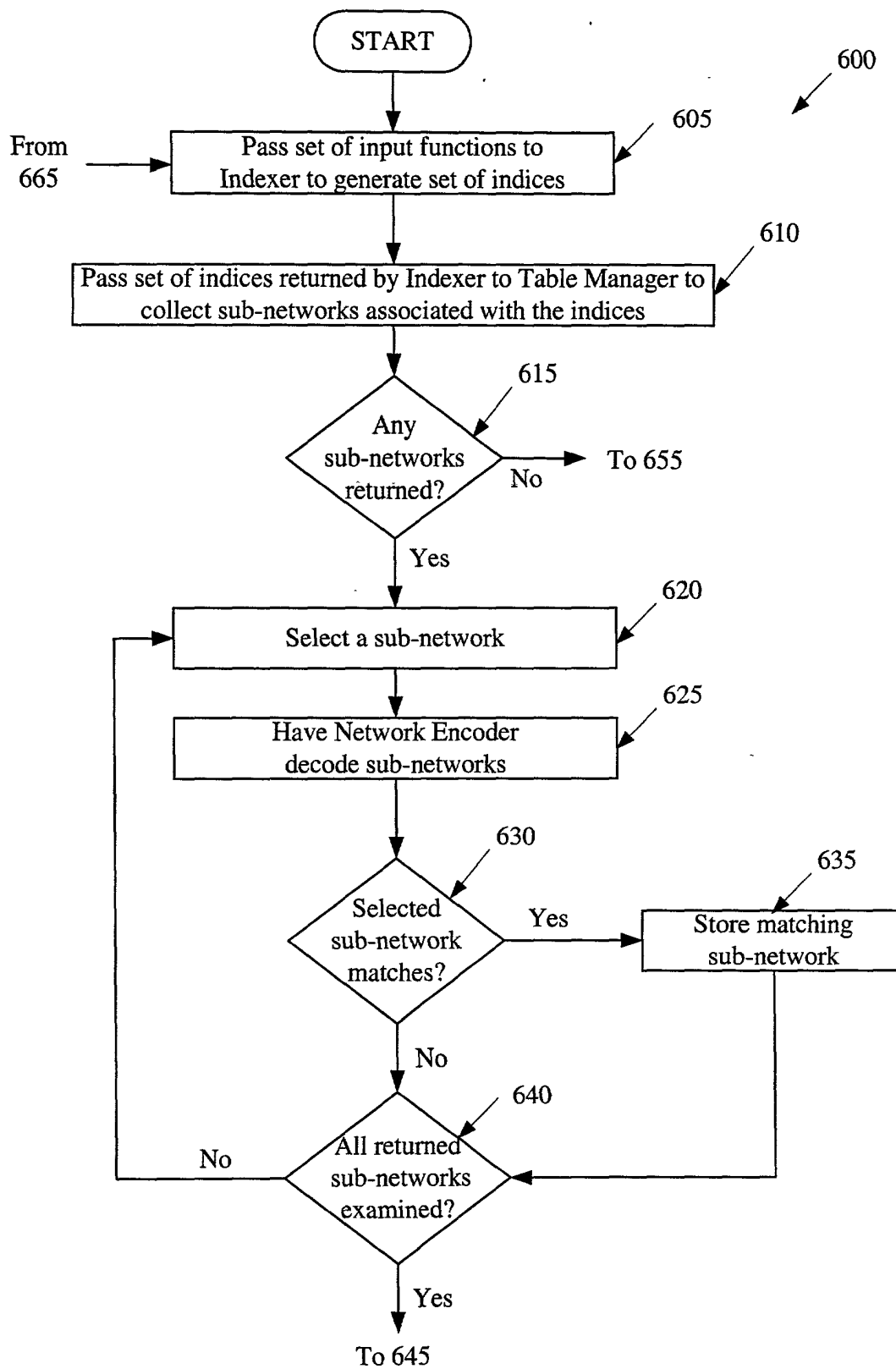


Figure 6A

Figure 6: Figure 6A
Figure 6B

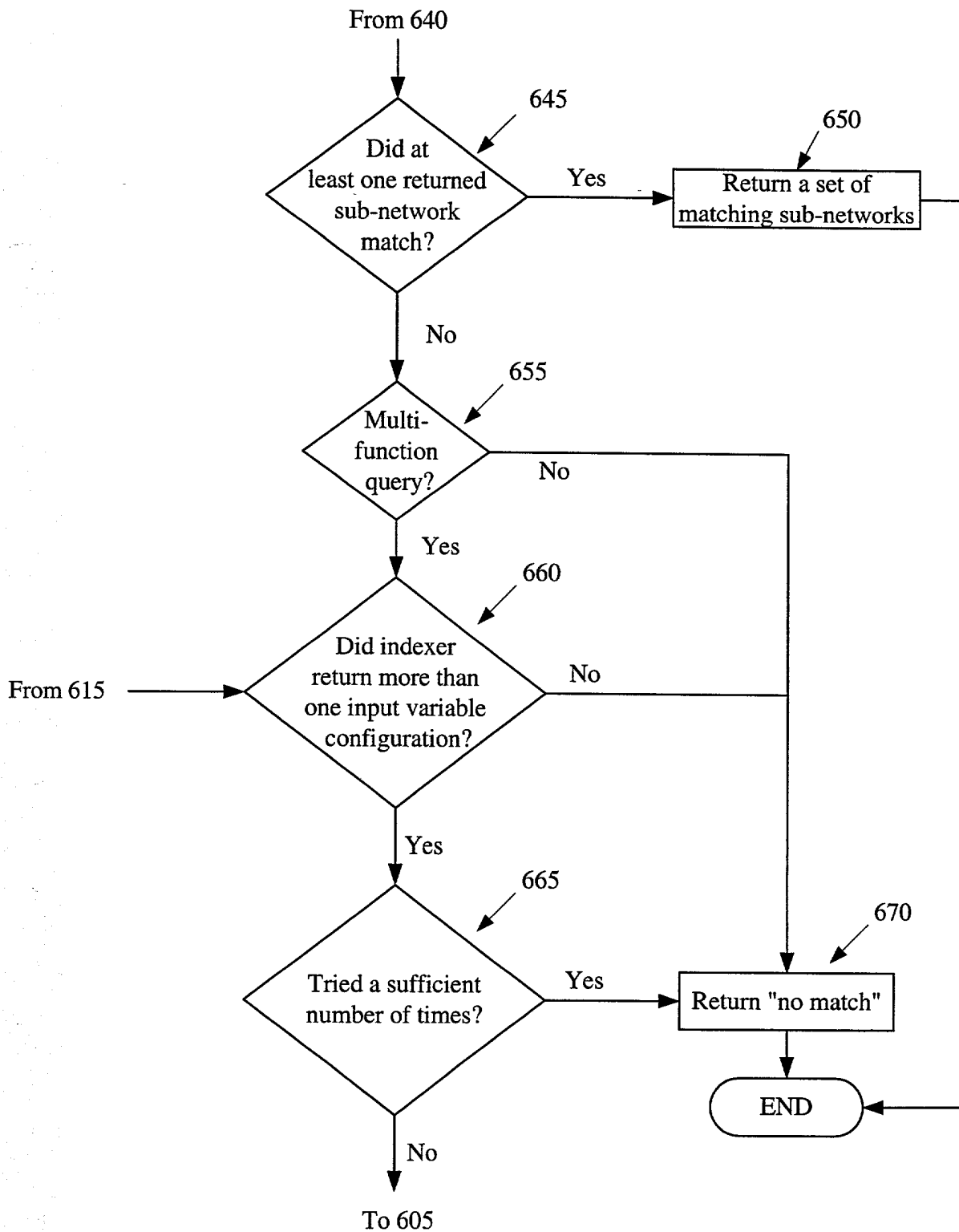


Figure 6B

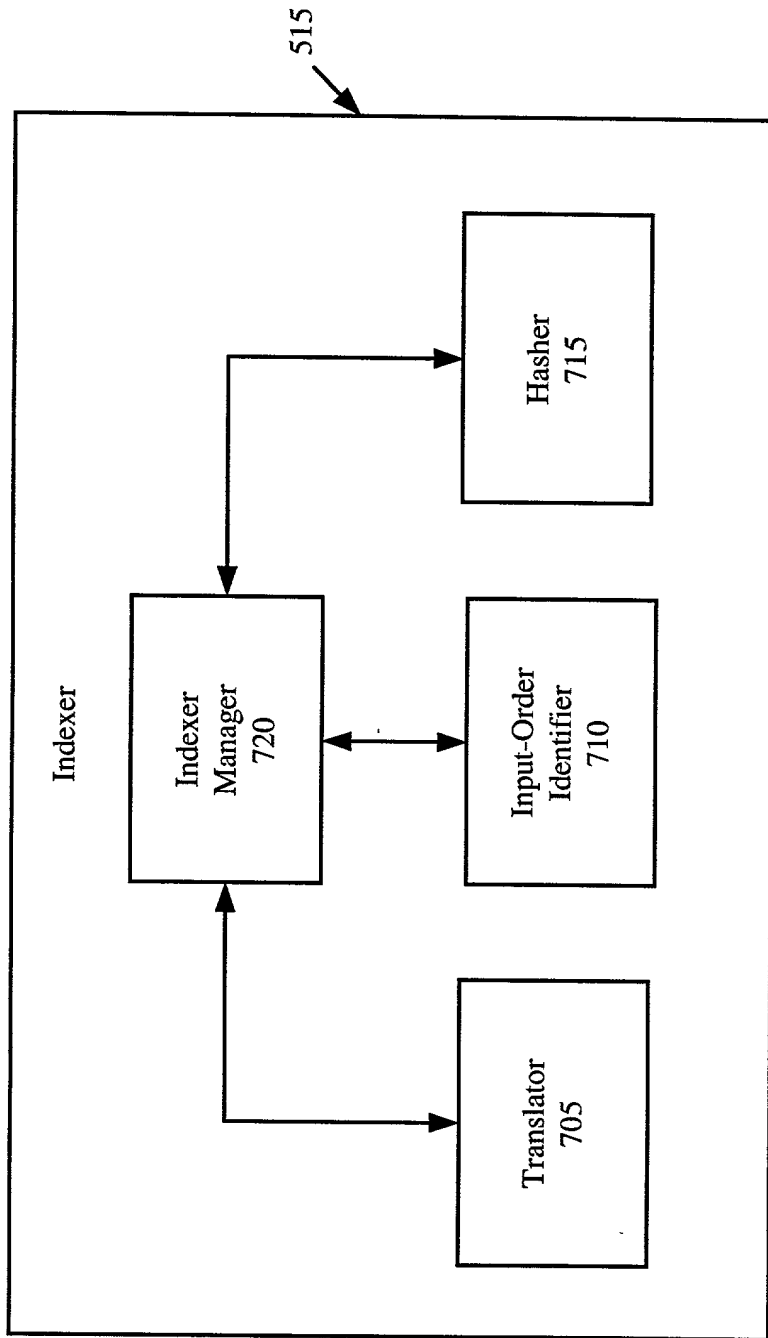


Figure 7

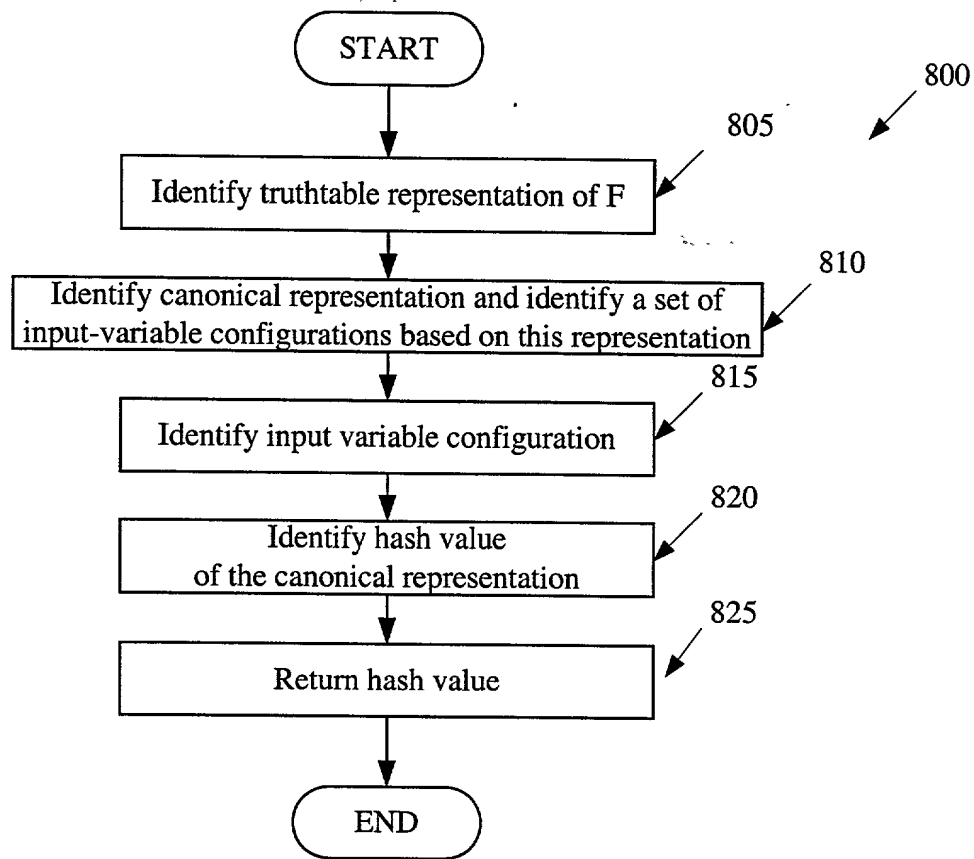


Figure 8

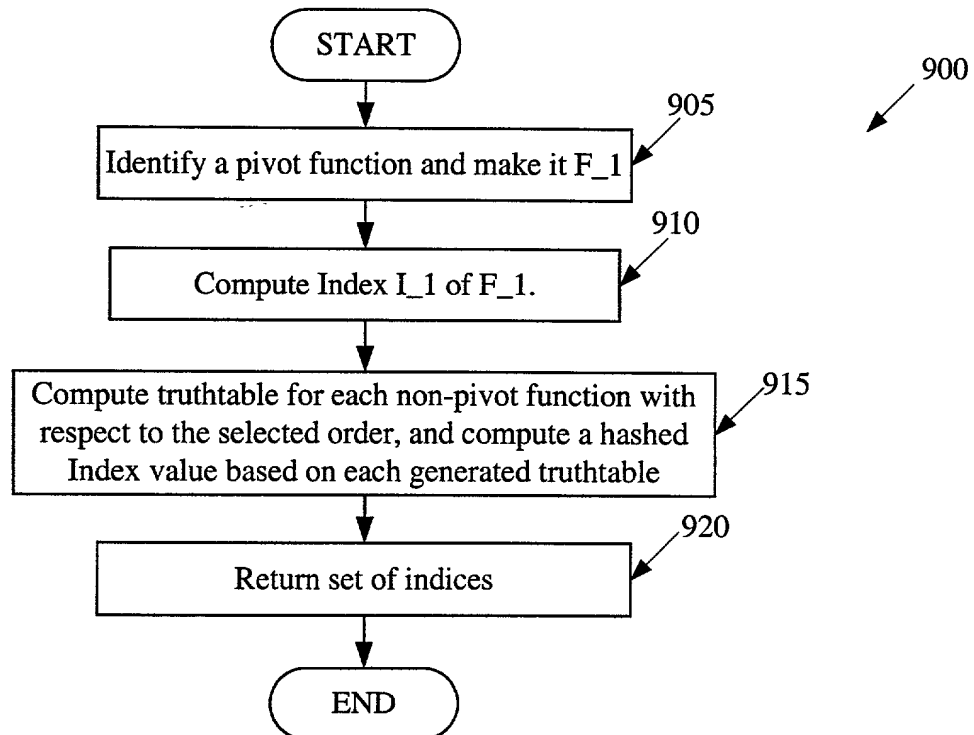


Figure 9

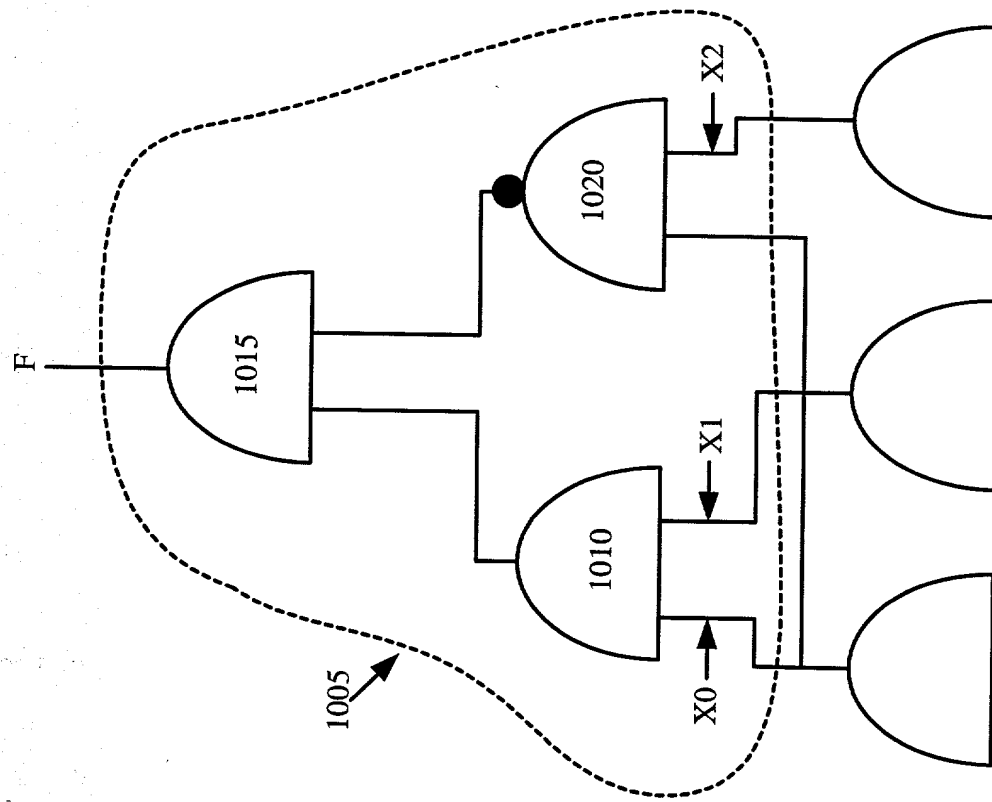


Figure 10

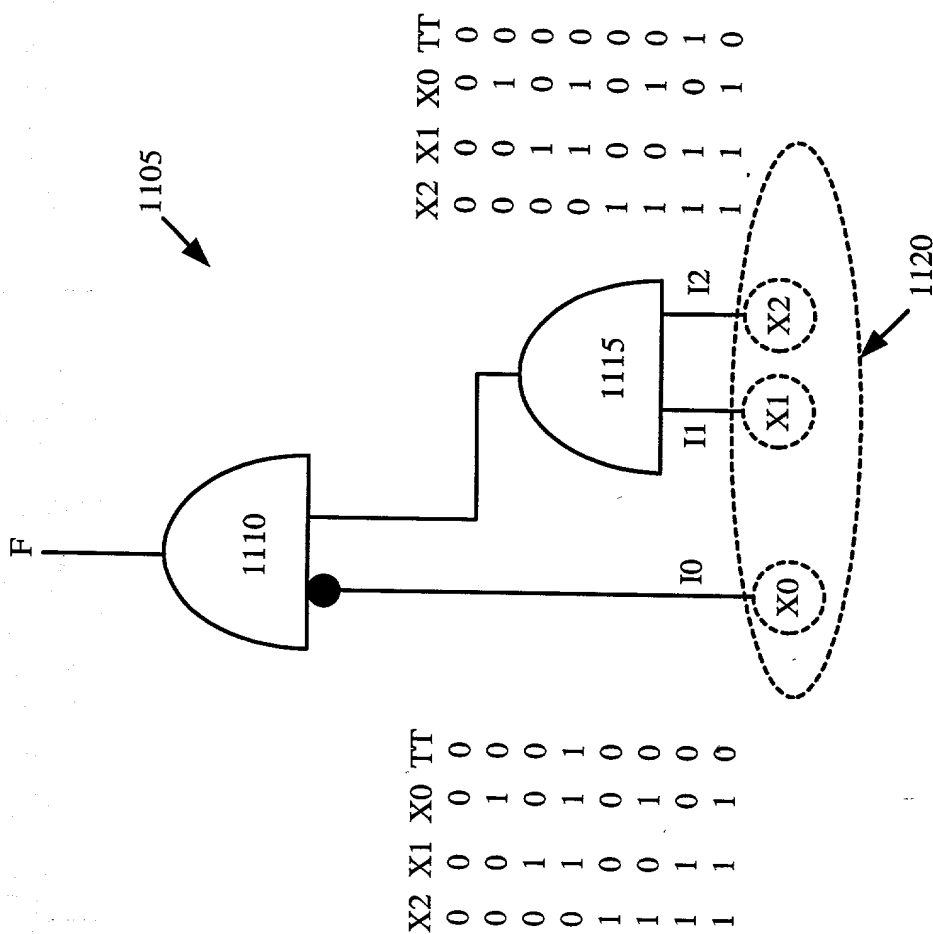
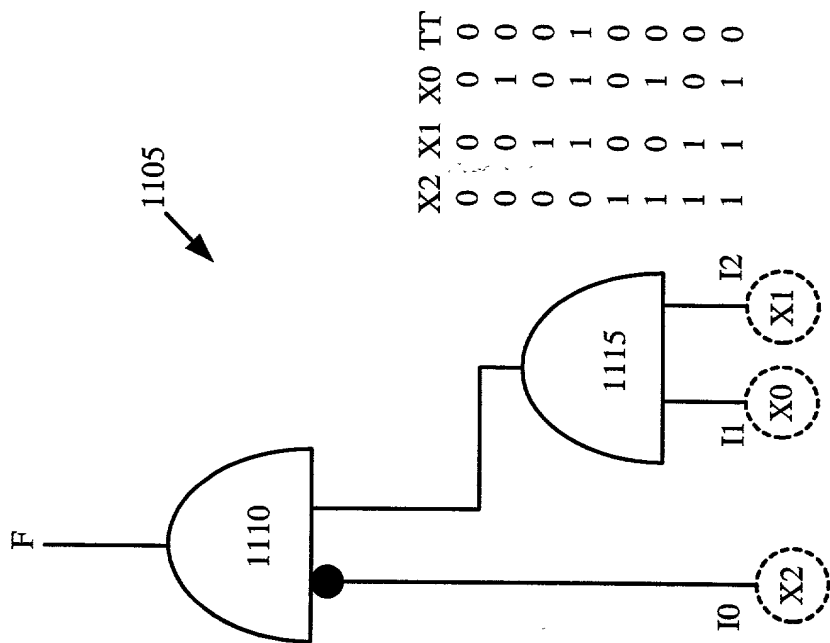
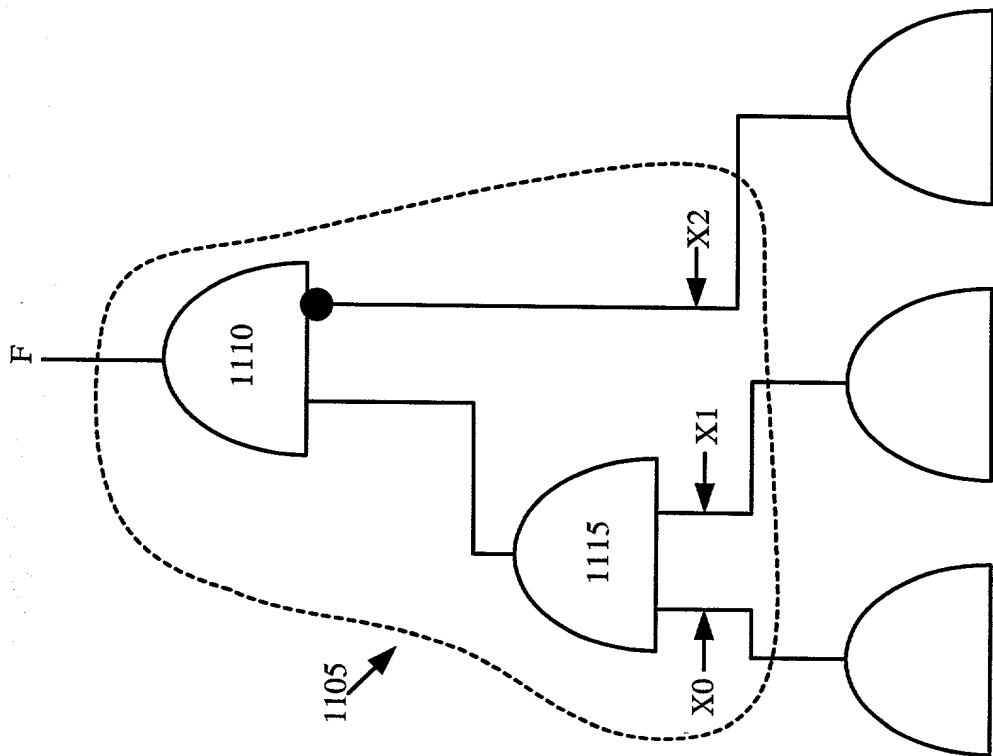


Figure 11



X2	X1	X0	TT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Figure 12



X2	X1	X0	TT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Figure 13

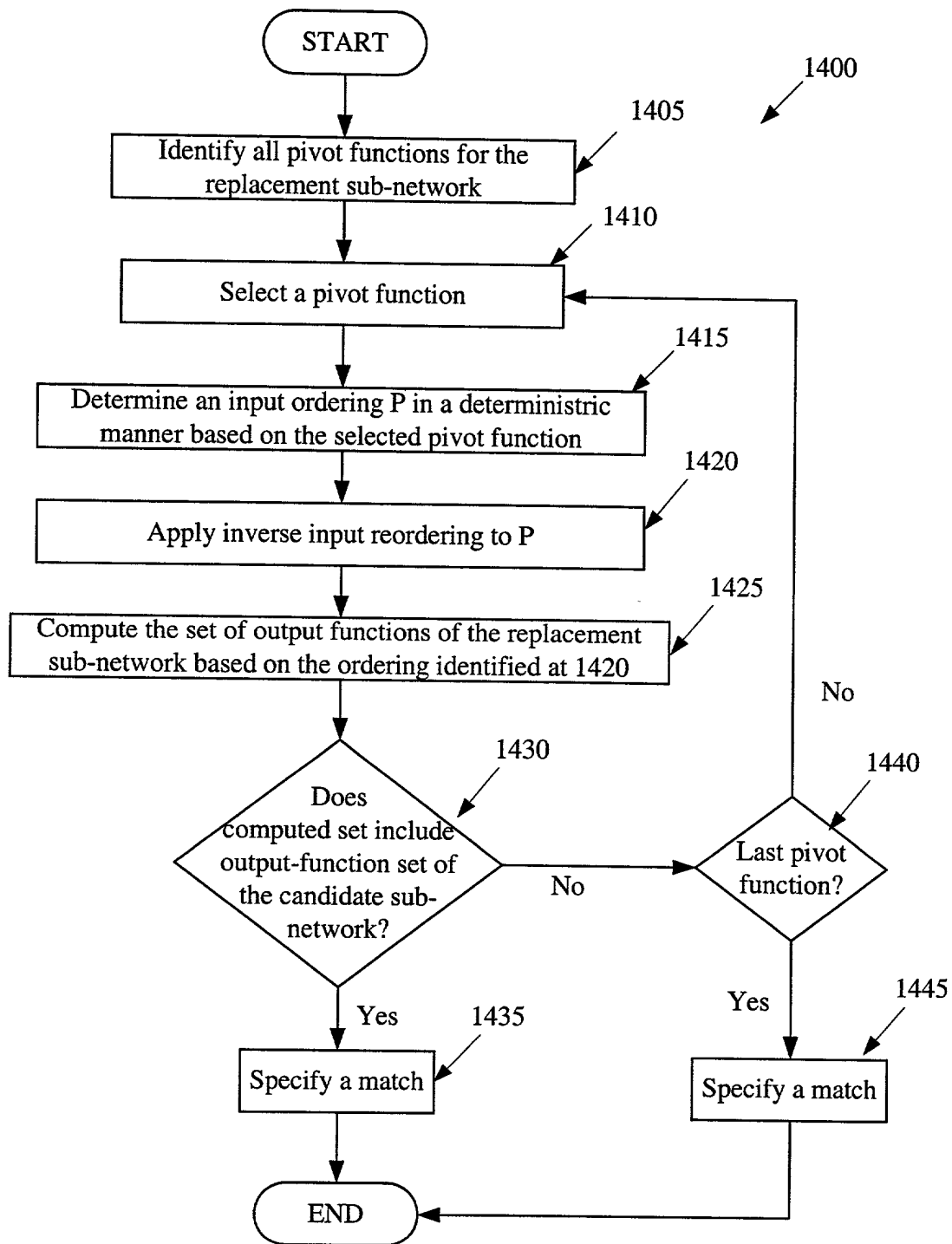


Figure 14

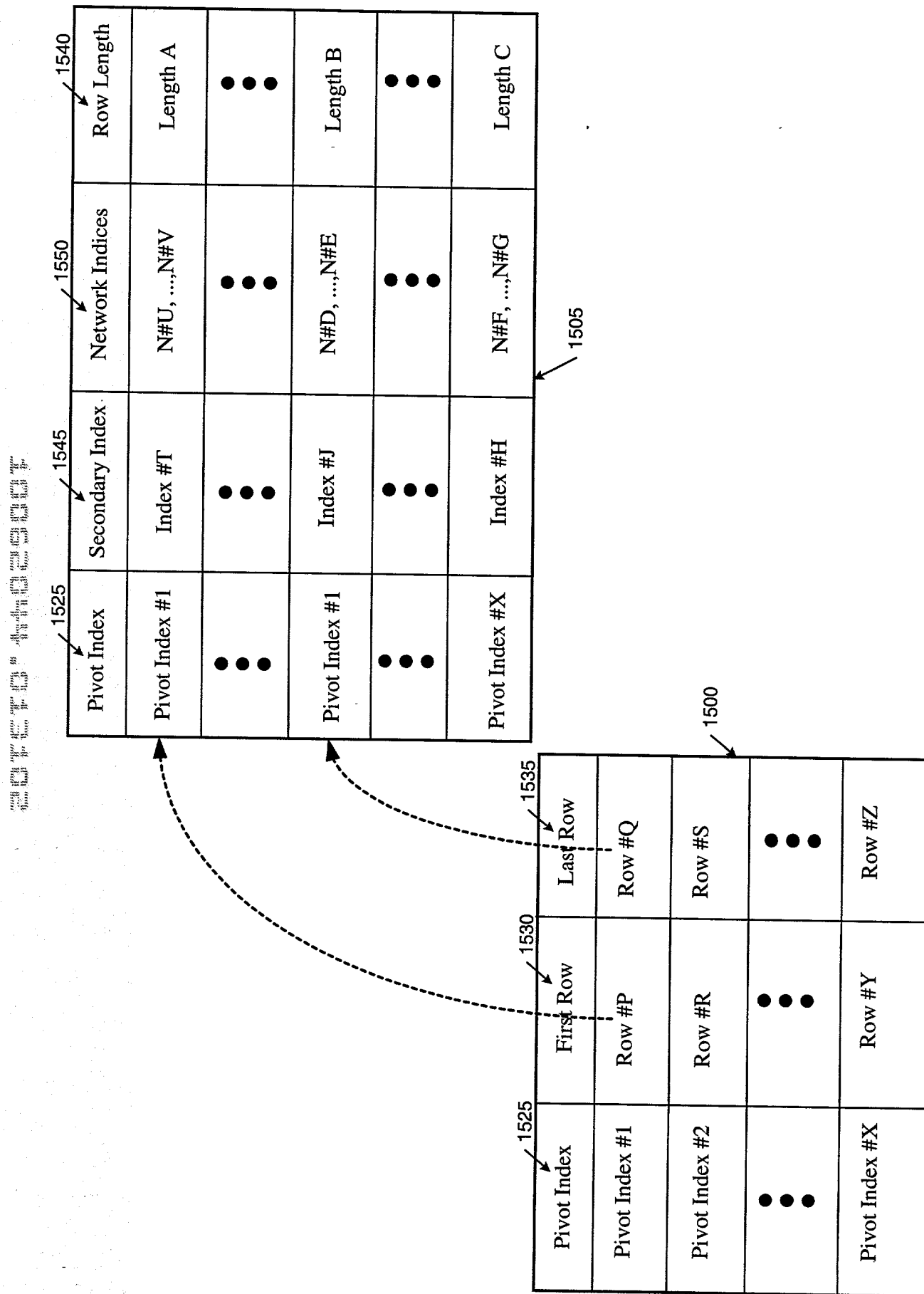


Figure 15

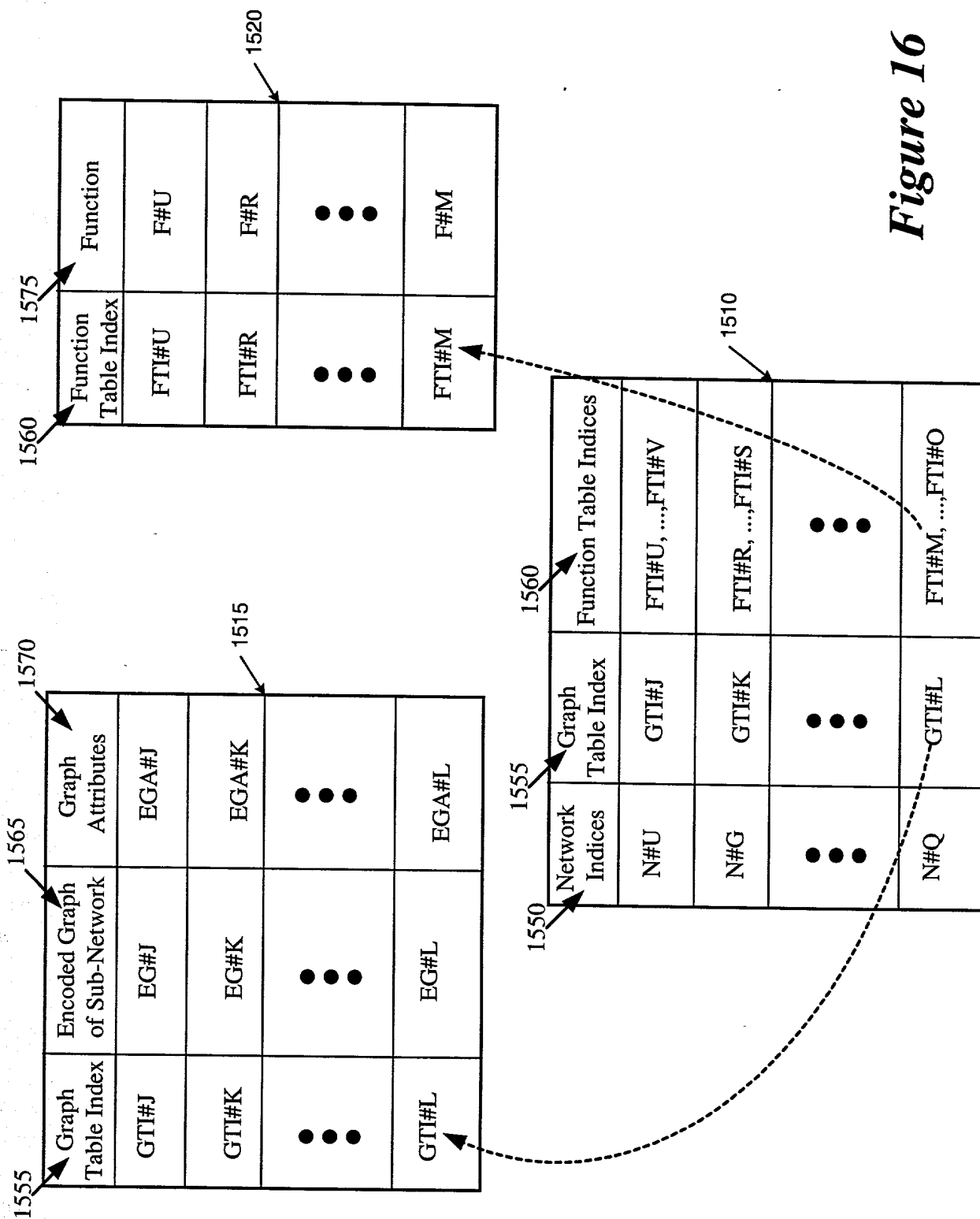


Figure 16

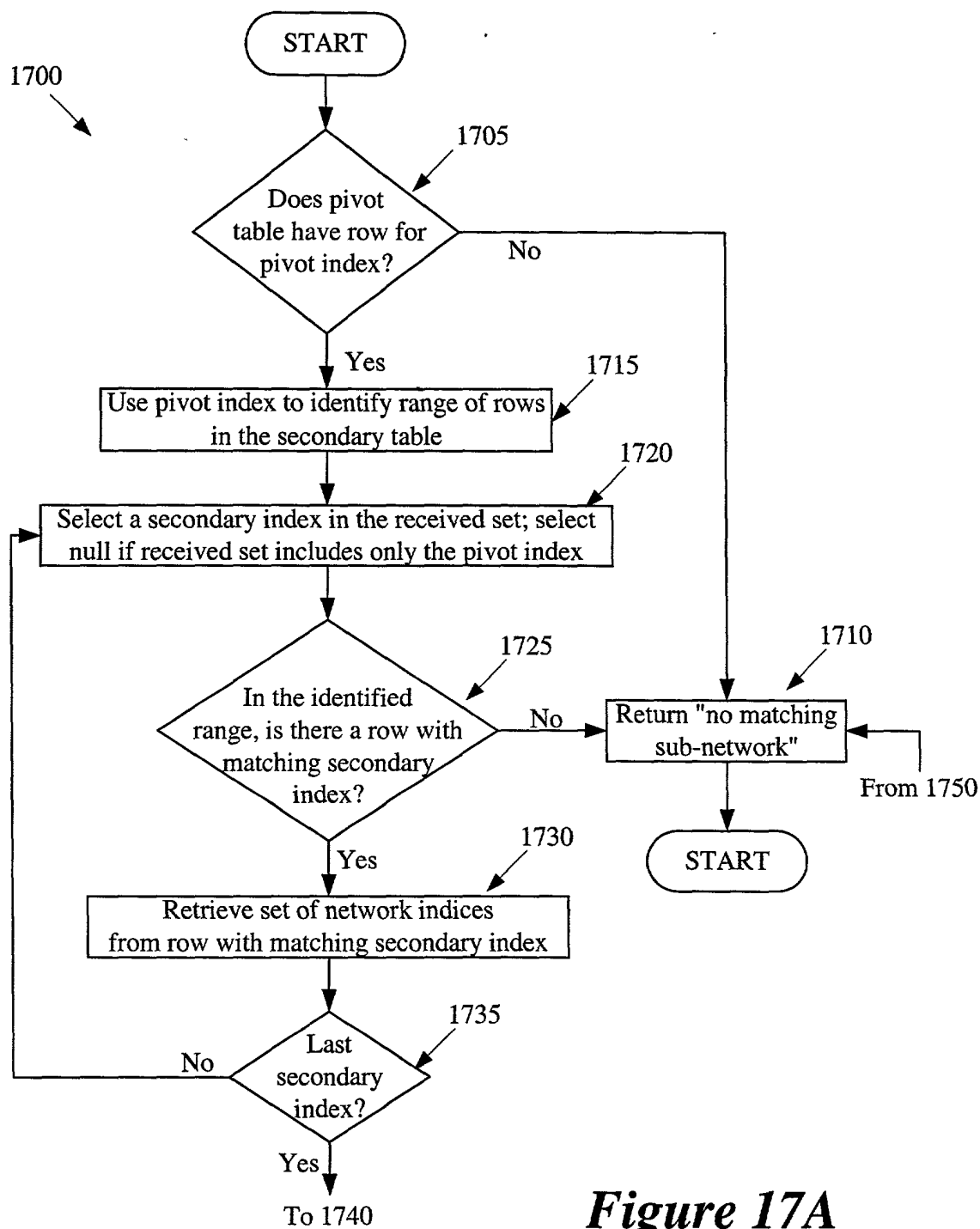


Figure 17A

Figure 17: Figure 17A
Figure 17B

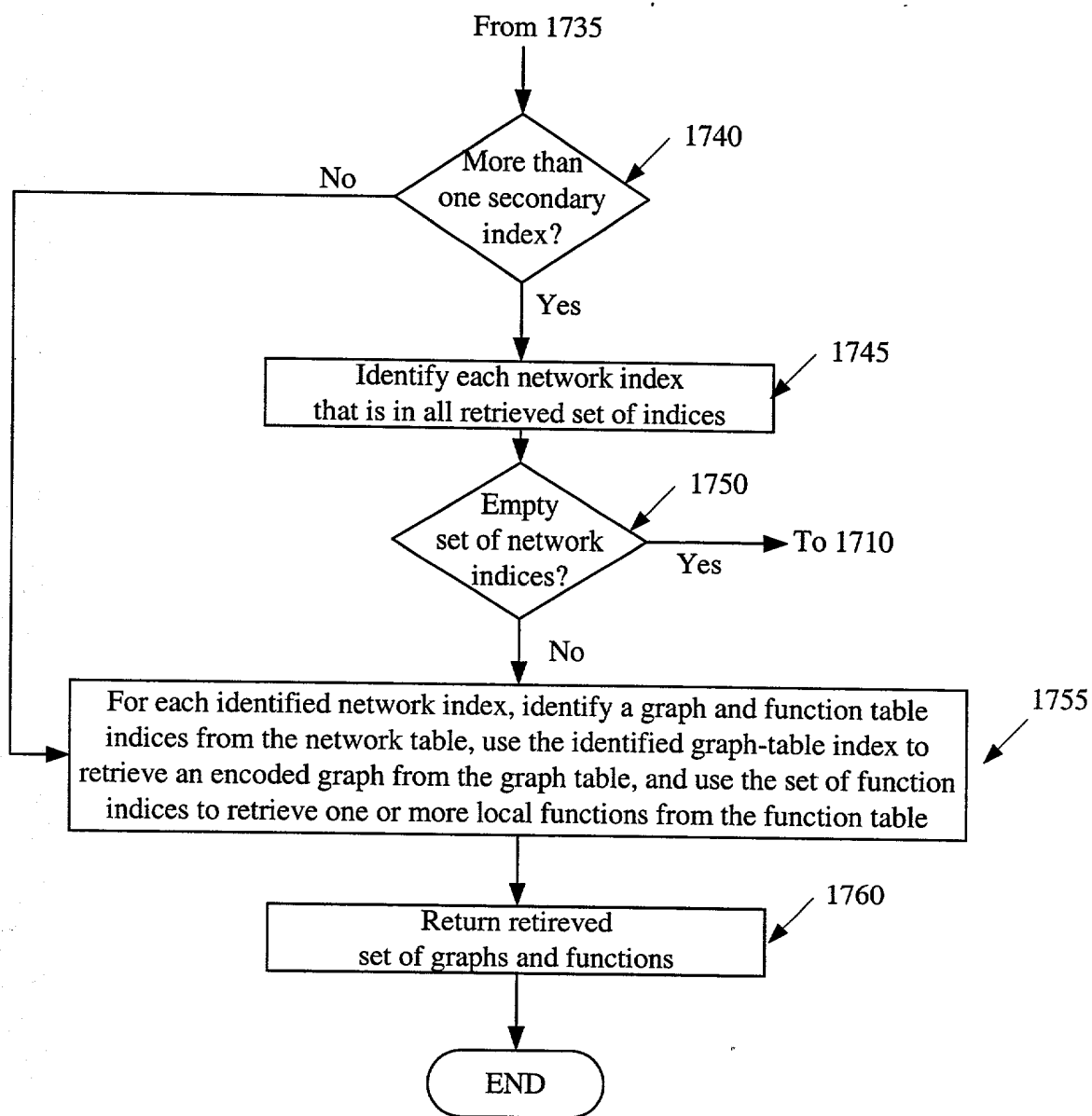


Figure 17B

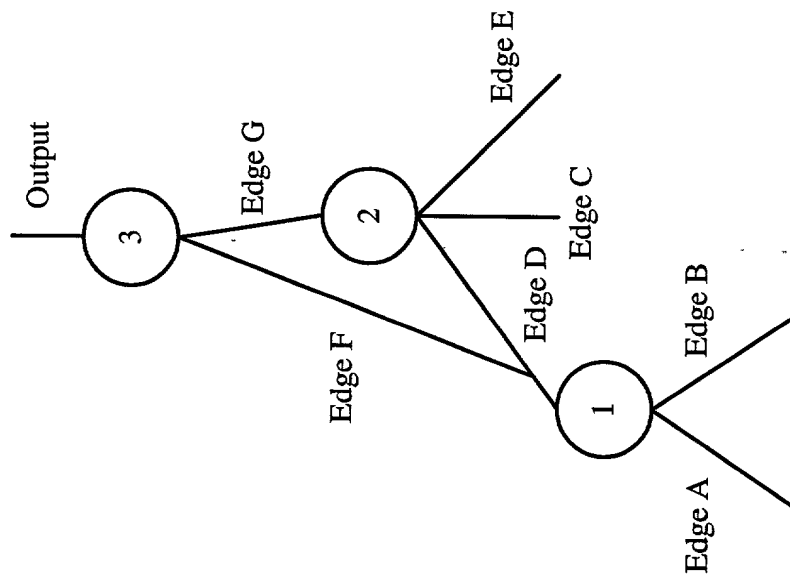


Figure 18

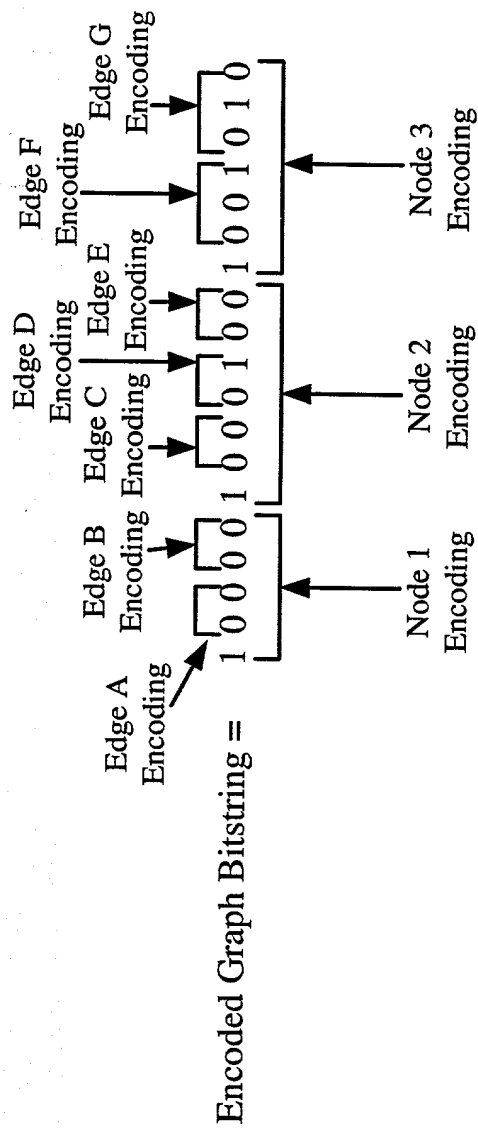


Figure 19

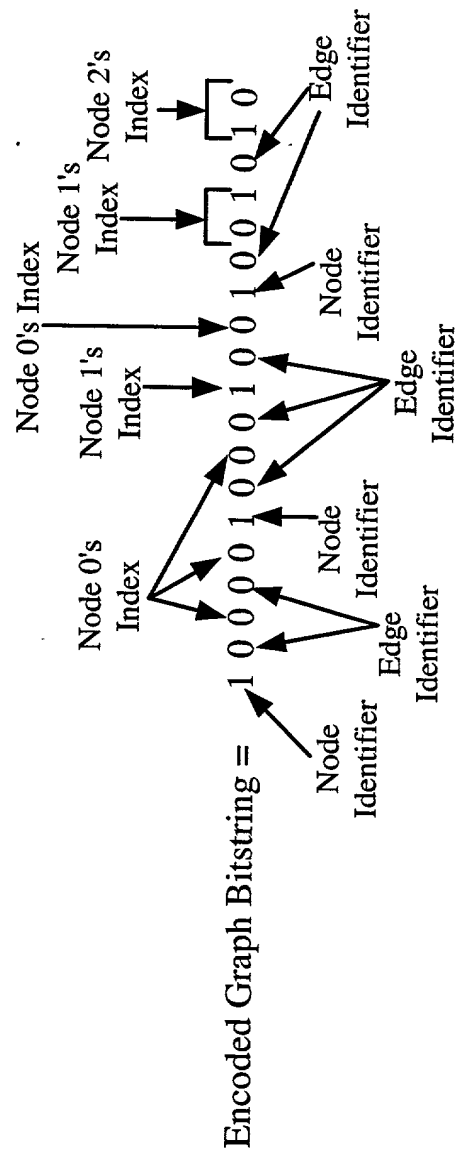


Figure 20

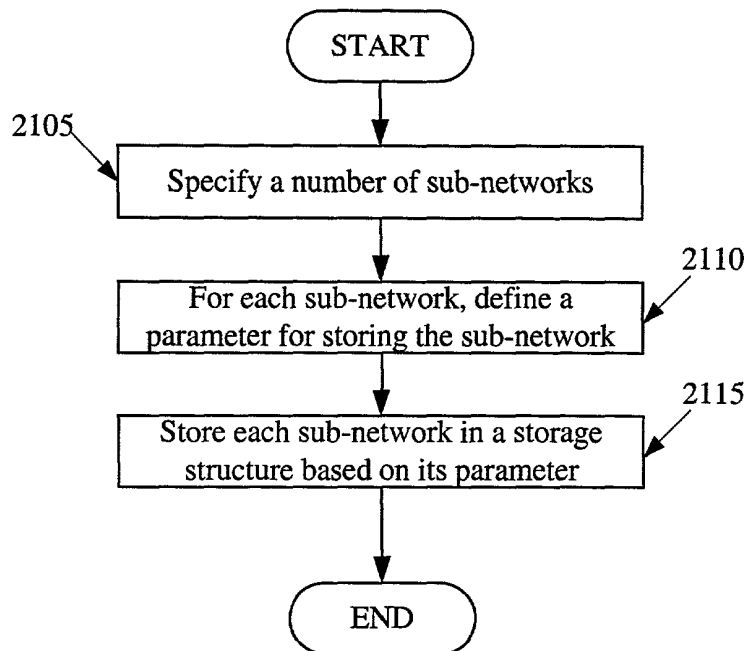


Figure 21

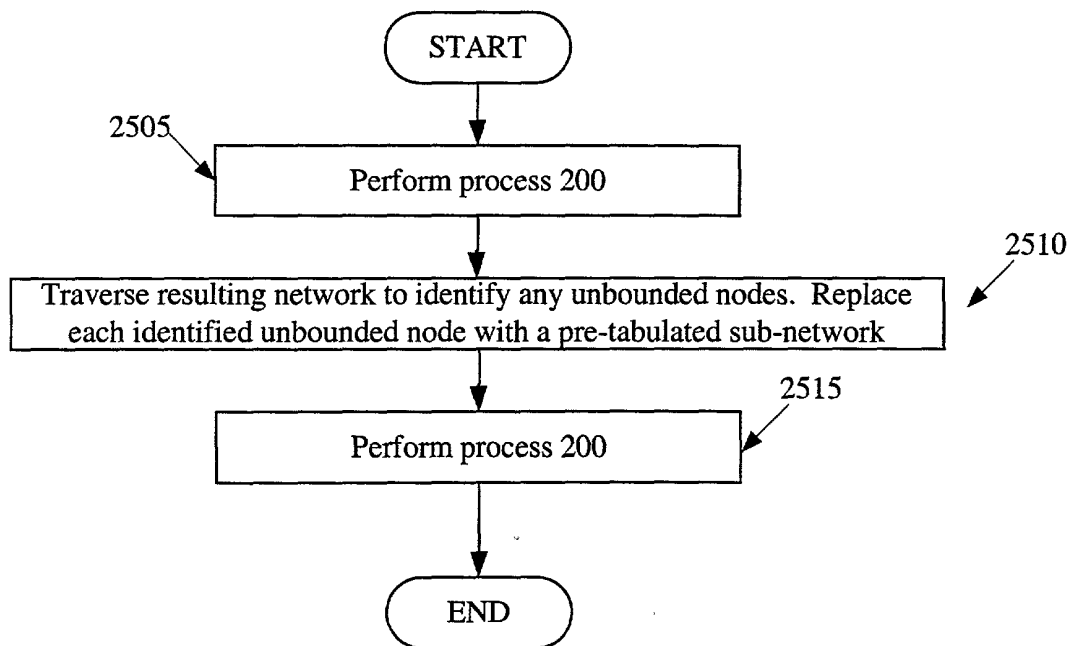


Figure 25

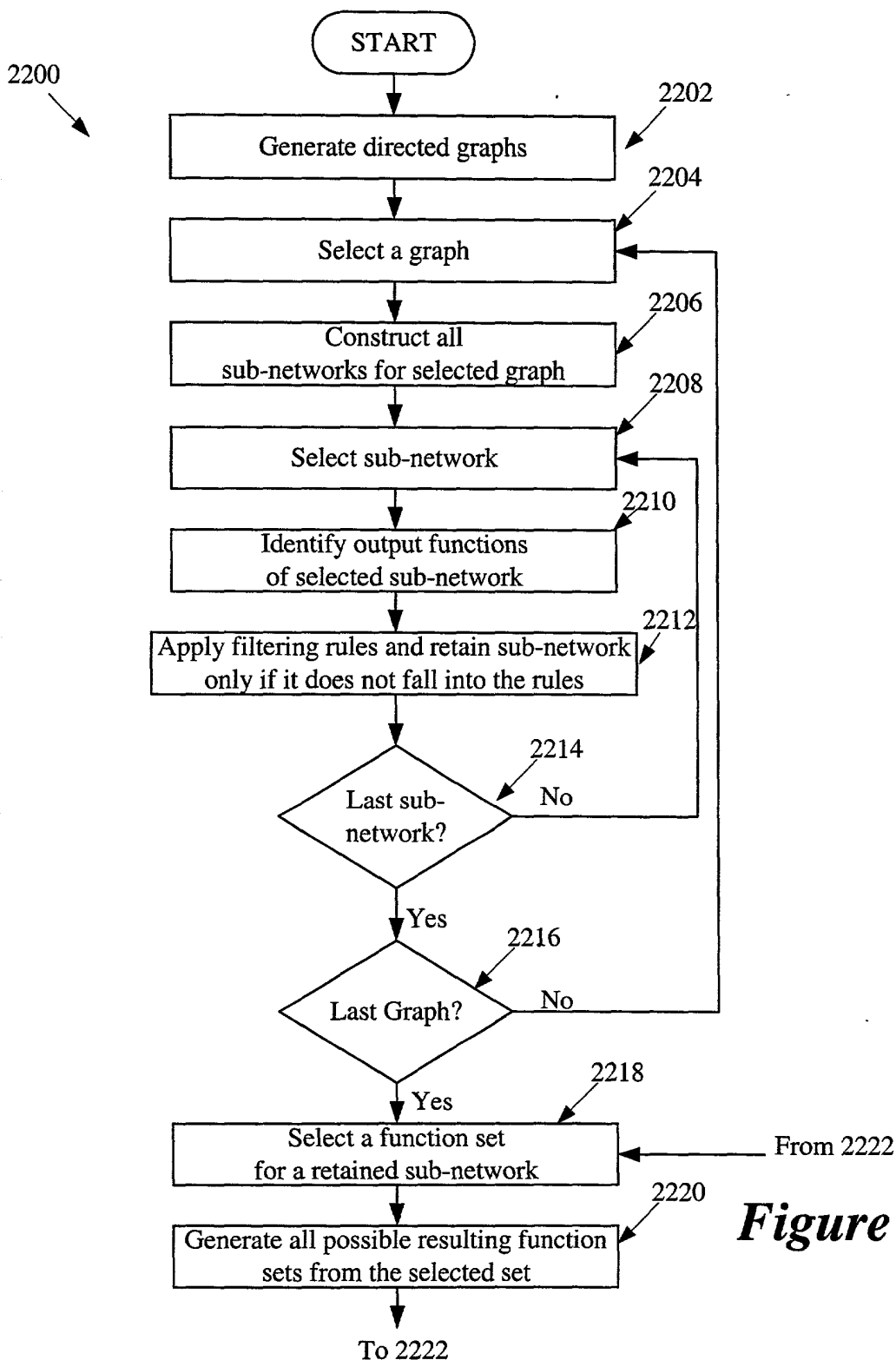


Figure 22A

Figure 22: Figure 22A
Figure 22B
Figure 22C

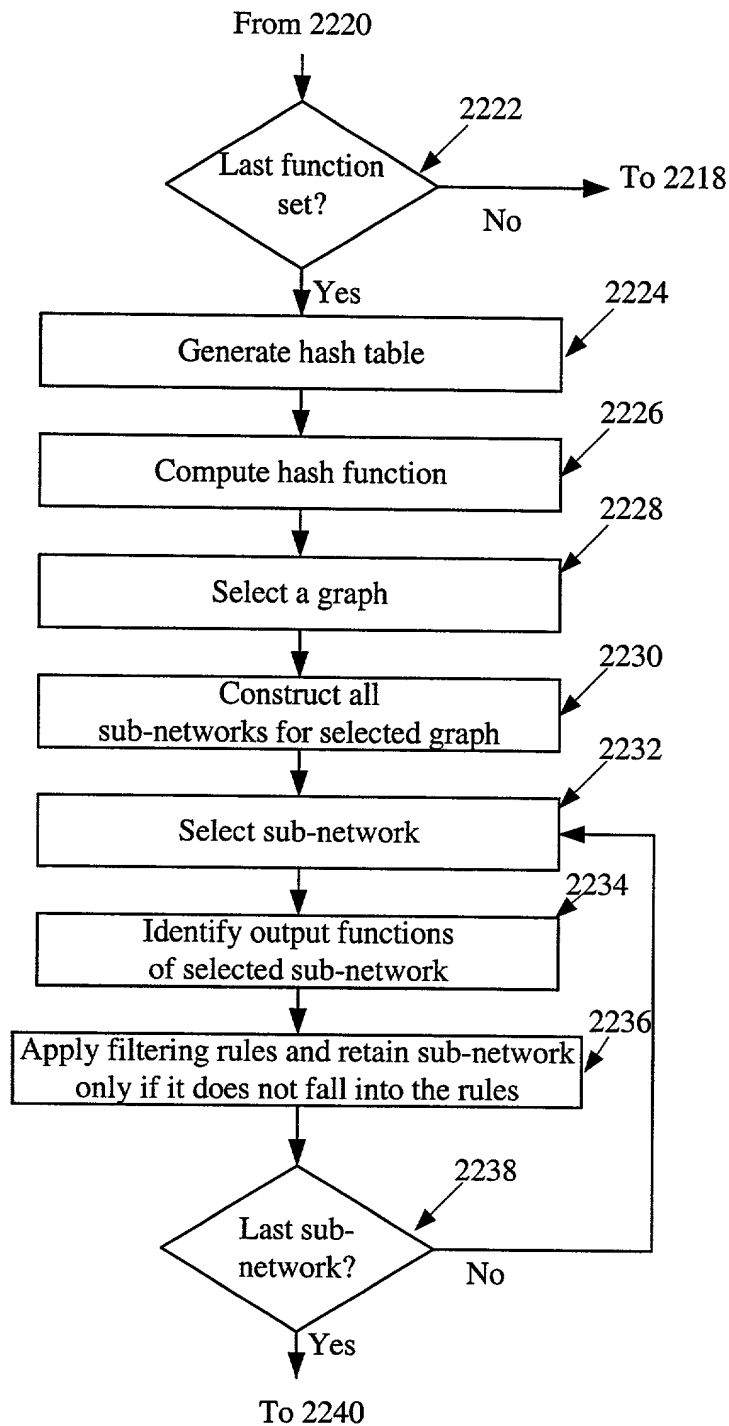


Figure 22B

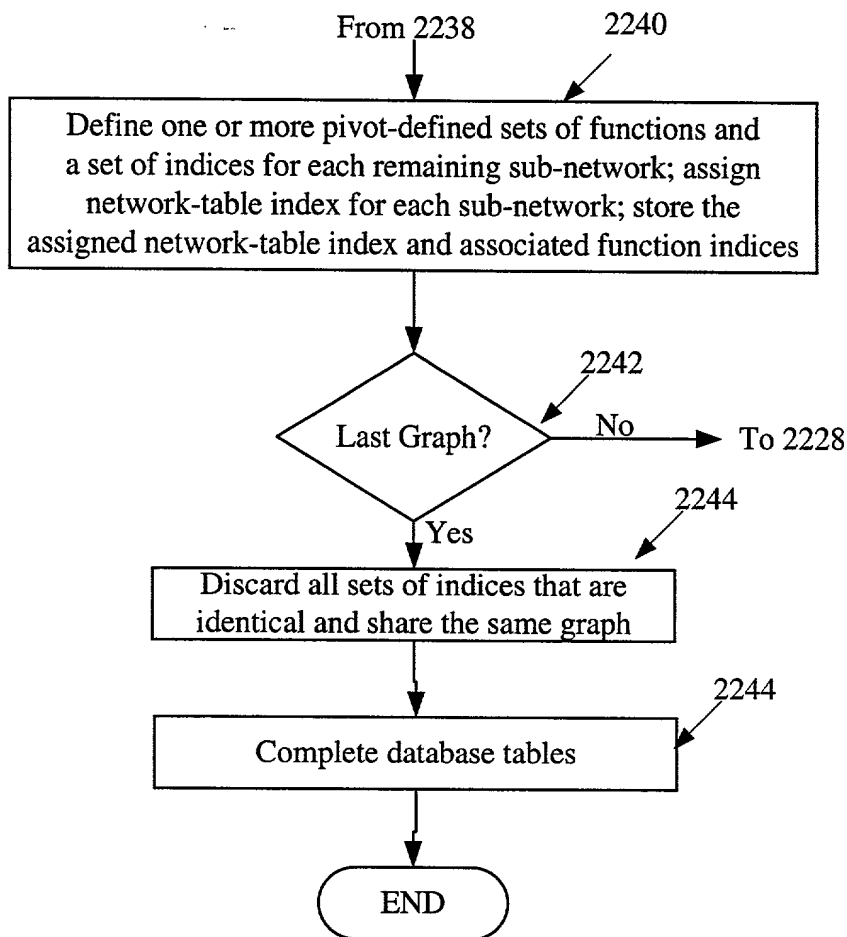


Figure 22C

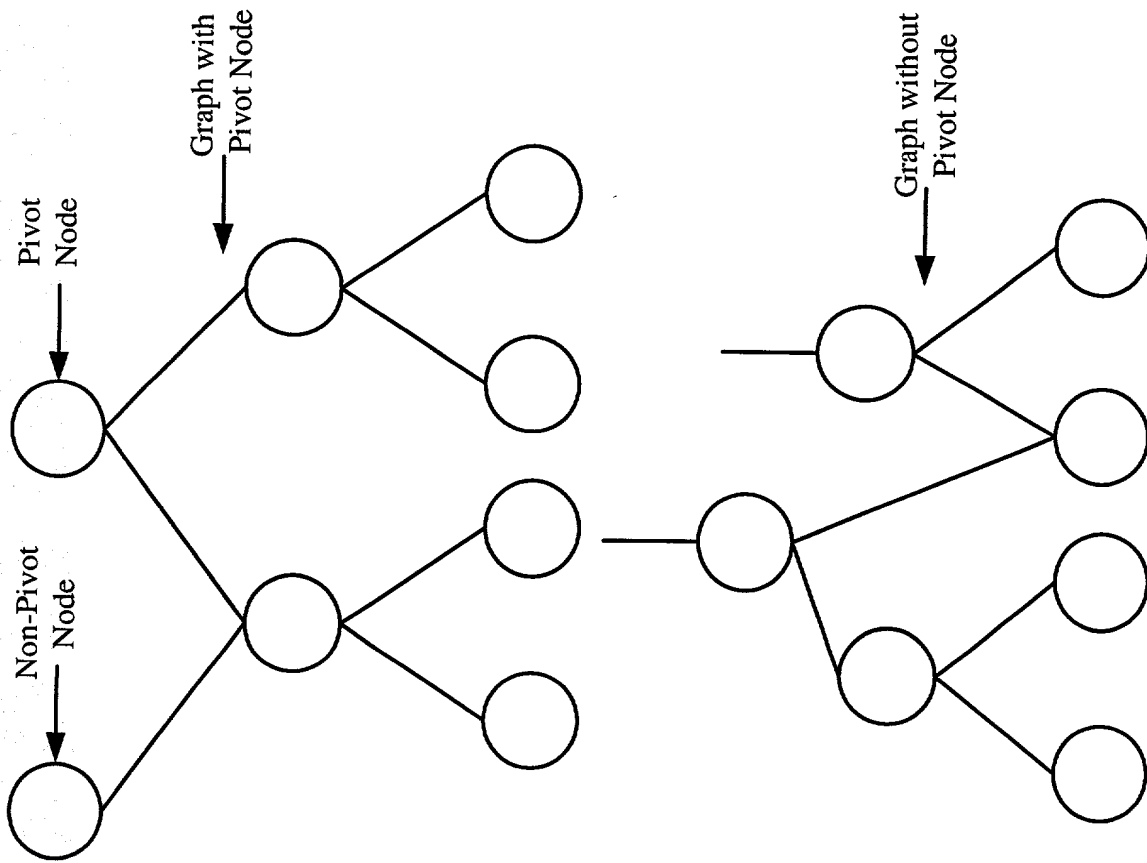


Figure 23

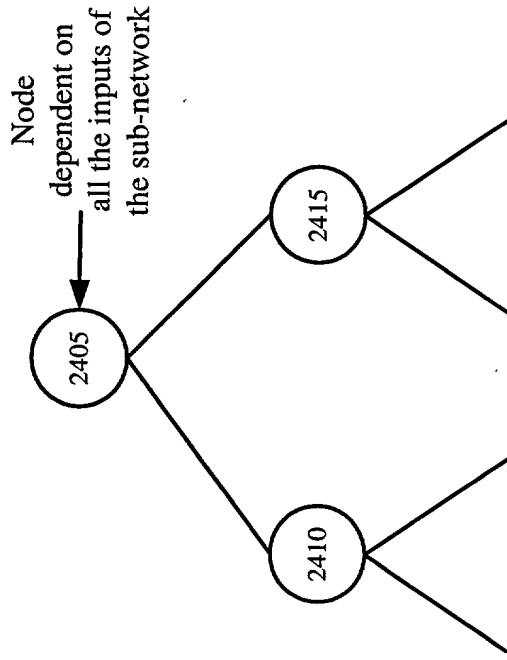


Figure 24

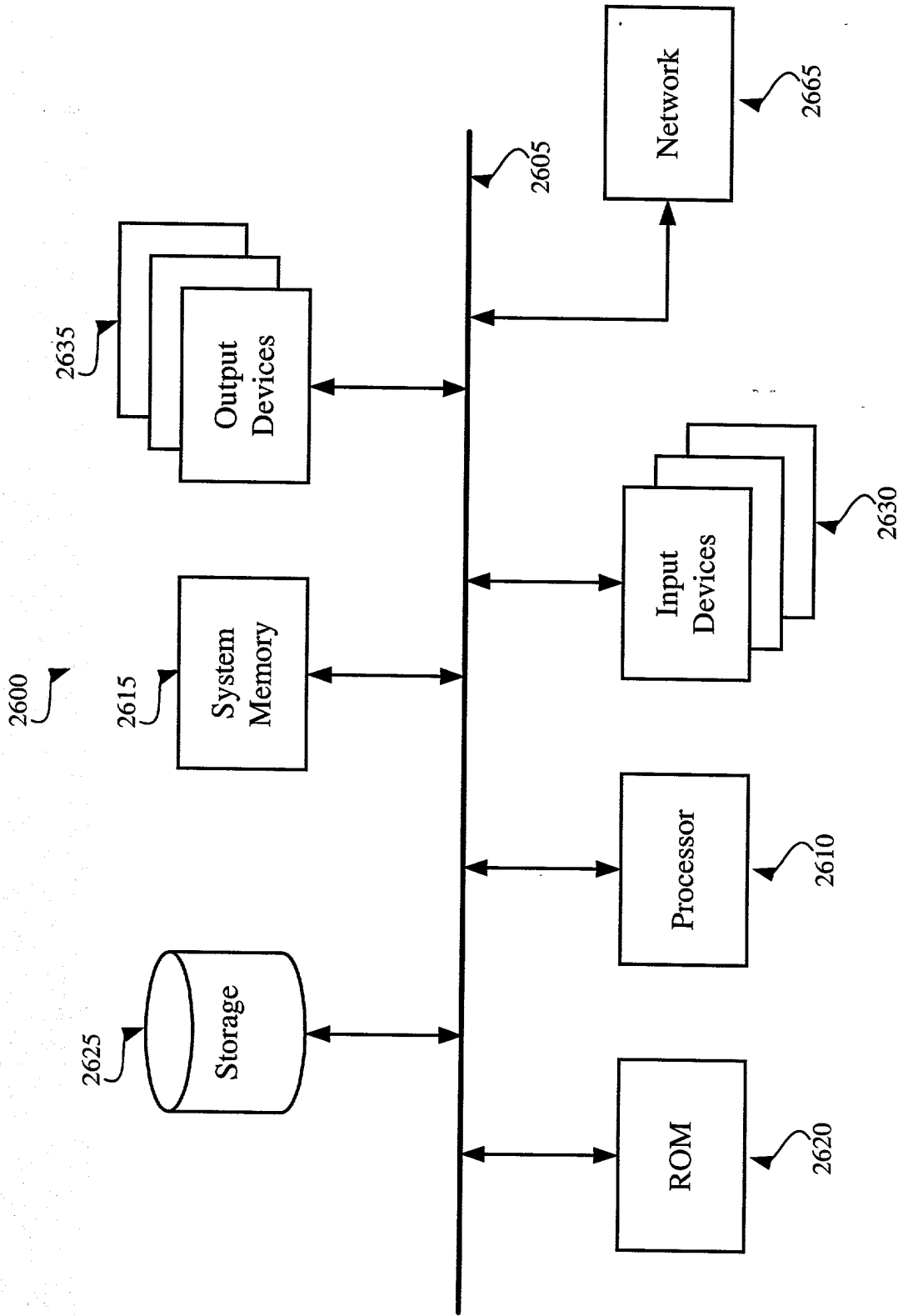


Figure 26